Aislyn Technologies Pvt Ltd

VLSI PROJECTS TITLE :

S. No	TITLES	TOOLS USED
1.	High-Speed Area-Efficient VLSI Architecture of Three-Operand Binary Adder.	Xilinx
2.	Design, FPGA implementation and statistical analysis of chaos-ring based dual entropy core true random number generator.	Xilinx
3.	A new family of CMOS inverter-based OTAs for biomedical and healthcare applications.	Tanner
4.	A Minimal-Cost Inherent-Feedback Approach for Low-Power MRF-Based Logic Gates.	Tanner
5.	Speed enhancement techniques for Clock-Delayed Dual Keeper Domino logic style.	Tanner
6.	Design Exploration of Energy-Efficient Accuracy -Configurable Dadda Multipliers With Improved Lifetime Based on Voltage Over-scaling.	Xilinx
7.	FPGA implementation of low power and high speed image edge detection algorithm.	Xilinx

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8.	Ultra efficient imprecise multipliers based on innovative 4:2approximate compressors	Xilinx
9.	FPGA implementation of XOR-MUX full adder based DWT for signal processing applications.	Xilinx
10.	DPL-Based Novel Time Equalized CMOS Ternary-to-Binary Converter.	Tanner
11.	DPL-Based Novel CMOS 1-Trit Ternary Full-Adder.	Tanner
12.	An Area-Efficient Variable-Size Fixed-Point DCT Architecture for HEVC Encoding	Xilinx
13.	Optimizing FPGA Logic Block Architectures for Arithmetic	Xilinx
14.	High-Speed Area-Efficient VLSI Architecture of Three-Operand Binary Adder	Xilinx
15.	Design of a Scalable Low-Power 1-bit Hybrid Full Adder for Fast Computation	Tanner
16.	Hybrid LUT/Multiplexer FPGA Logic Architectures	Xilinx
17.	Fault Tolerant Parallel FFTs Using Error Correction Codes and Parseval Checks	Xilinx
18.	Flexible DSP Accelerator Architecture Exploiting Carry-Save Arithmetic	Xilinx
19.	High-Performance NB-LDPC Decoder With Reduction of	Xilinx

	Message Exchange	
20.	High-Speed and Energy-Efficient Carry Skip Adder Operating Under a Wide Range of Supply Voltage Levels	Xilinx
21.	Low-Power Split-Radix FFT Processors Using Radix-2 Butterfly Units	Xilinx
22.	Input-Based Dynamic Reconfiguration of Approximate Arithmetic Units for Video Encoding	Xilinx
23.	The VLSI Architecture of a Highly Efficient Deblocking Filter for HEVC Systems	Xilinx
24.	VLSI design of low-cost and high-precision fixed-point reconfigurable FFT processors	Xilinx
25.	A Variable-Clock-Cycle-Path VLSI Design of Binary Arithmetic Decoder for H.265/HEVC	Xilinx
26.	Low Overhead Warning Flip-Flop Based on Charge Sharing for Timing Slack Monitoring	Tanner
27.	An area efficient low-voltage 6-T SRAM cell using stacked silicon Nano wires	Tanner
28.	Read Static Noise Margin Decrease of 65-nm 6-T SRAM Cell Induced by Total Ionizing Dose	Tanner
29.	A variable size FFT hardware accelerator based on matrix	Xilinx

	transposition	
30.	An FPGA-Based Cloud System for Massive ECG Data Analysis	Xilinx
31.	An Improved Signed Digit Representation Approach for Constant Vector Multiplication	Xilinx
32.	A High-Performance FIR Filter Architecture for Fixed and Reconfigurable Applications	Xilinx
33.	An Efficient Hardware Implementation of Canny Edge Detection Algorithm	Xilinx
34.	A Modified Partial Product Generator for Redundant Binary Multipliers	Xilinx
35.	Built-in Self Testing of FPGAs	Xilinx
36.	Area-Efficient Pipelined VLSI Architecture for Polar Decoder	Xilinx
37.	Area and Power Efficient 64-Bit Booth Multiplier	Xilinx
38.	A Low-Cost High-Performance VLSI Architecture for Image Scaling in Multimedia Applications	Xilinx
39.	VLSI Architecture for High-Performance Wallace Tree Encoder	Xilinx
40.	VLSI Implementation of Reed Solomon Codes	Xilinx

41.	A Design Implementation and Comparative Analysis of Advanced Encryption Standard (AES) Algorithm on FPGA	Xilinx
42.	Design of Modified Dual-CLCG Algorithm for Pseudo-Random Bit Generator	Xilinx
43.	Efficient Operand Divided Hybrid Adder for Error Tolerant Applications	Xilinx
44.	Design and Synthesis of a 256-Point Radix-2 DIT FFT Core with Design Ware Library using Fixed-Point Number Representation	Xilinx
45.	Approach for Implementation of Vending Machine through Verilog HDL	Xilinx
46.	Design and Performance Analysis of Various 32-bit Hybrid Adders using Verilog	Xilinx
47.	A Programmable and Parameterizable Reseeding Linear Feedback Shift Register	Xilinx
48.	Design and Synthesis of a 256-Point Radix-2 DIT FFT Core with Design Ware Library using Fixed-Point Number Representation	Xilinx
49.	Fully Automated Traffic Light Controller system for a four-way intersection using Verilog	Xilinx

50.	A Novel Ultra-Compact FPGA-Compatible TRNG Architecture Exploiting Latched Ring Oscillators	Xilinx